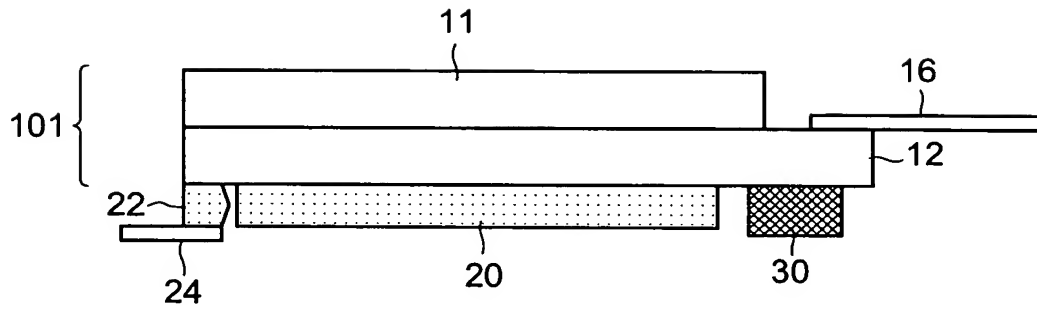
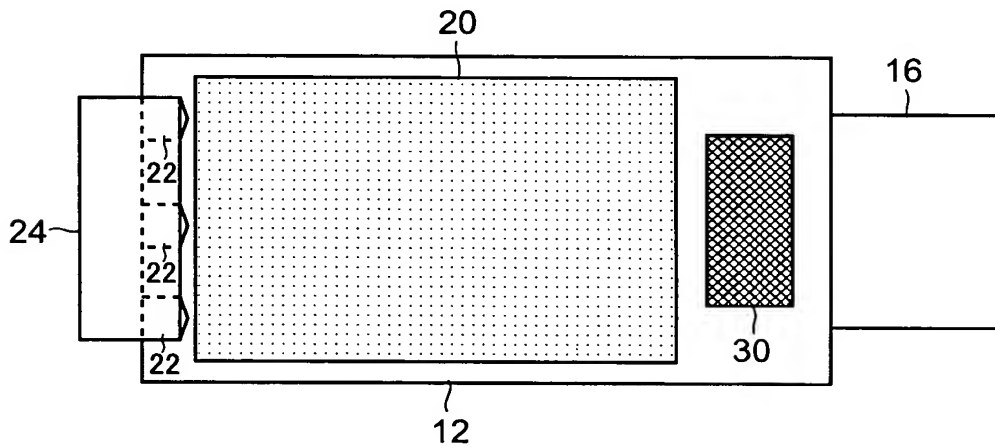


*Fig. 1**Fig. 2**Fig. 3*

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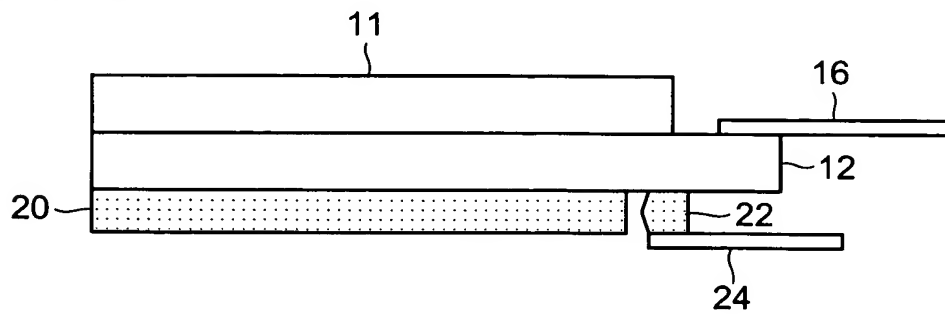
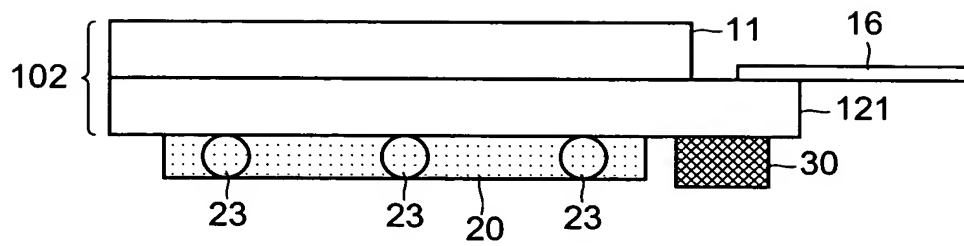
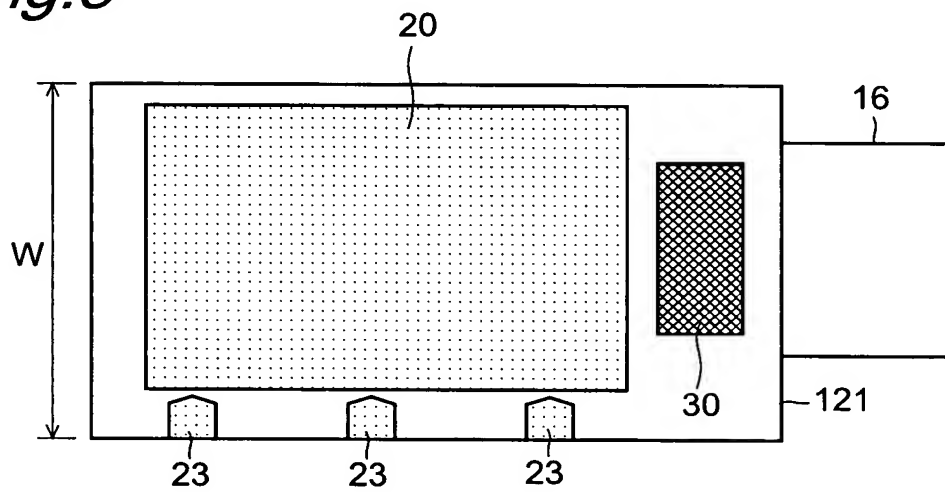
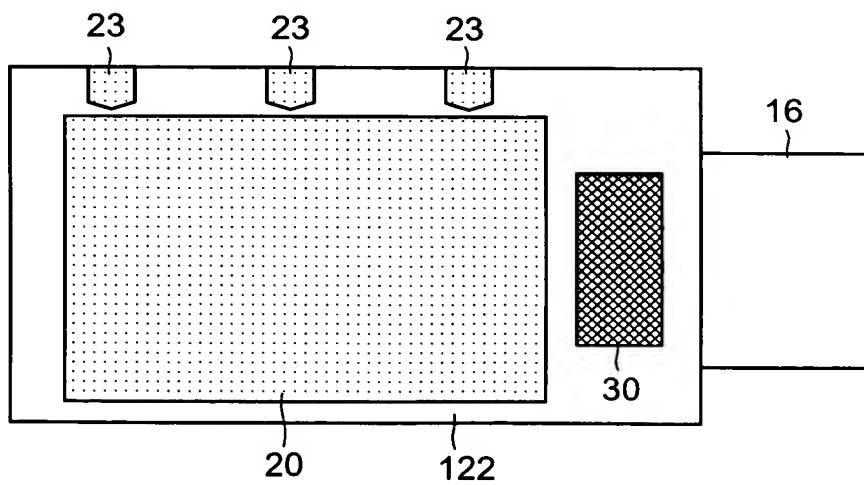
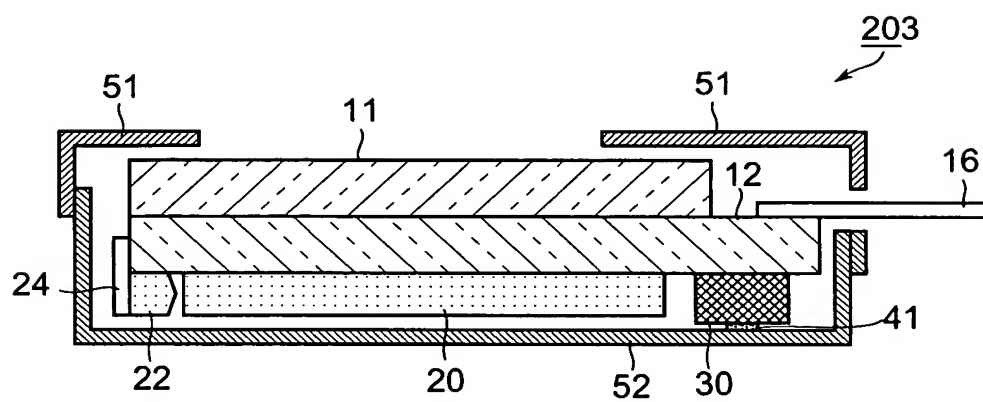


Fig. 1 is a cross-sectional view of a semiconductor device. The device consists of a substrate 10 with a top layer 11 and a bottom layer 12. A central region 20 is filled with a material 21. The device is surrounded by a frame 16. A cross-section line A-A is indicated at the bottom.

*Fig. 7**Fig. 8**Fig. 9*

*Fig. 10*

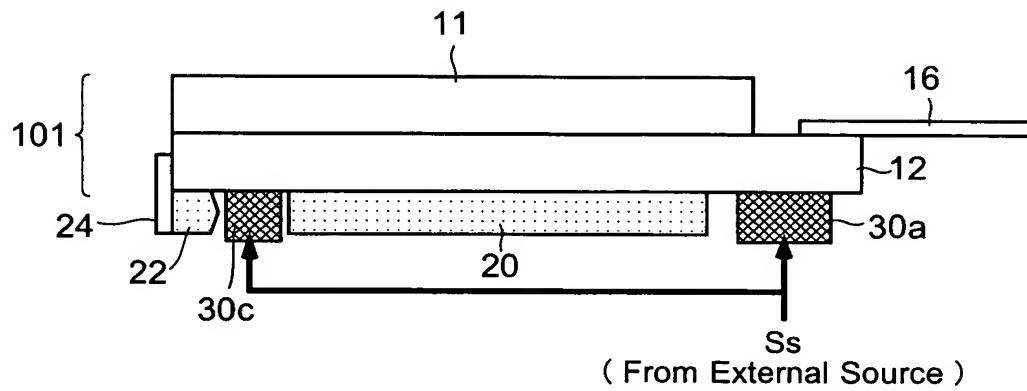
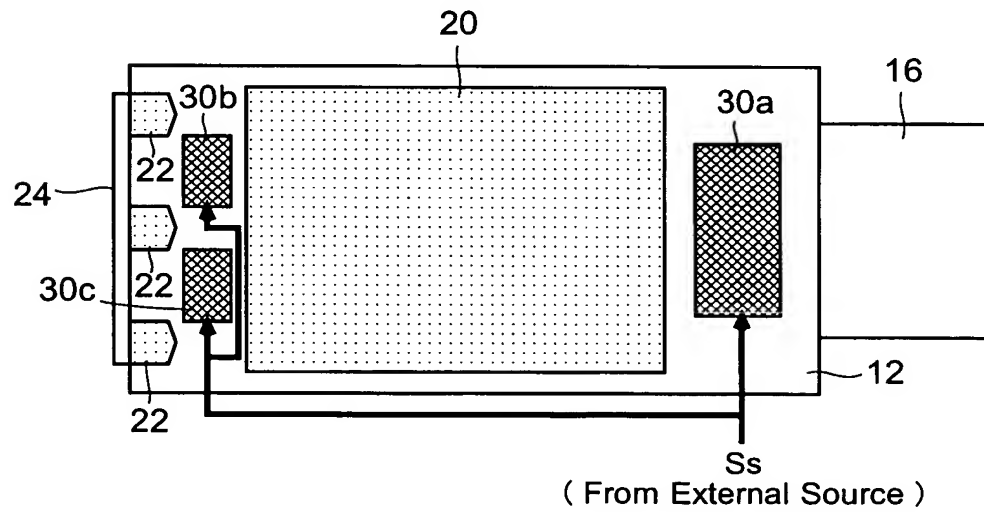
*Fig. 11**Fig. 12*

Fig. 1 is a cross-sectional view of a semiconductor device. The device includes a substrate 11. A top layer 12 is formed on the substrate 11. A gate stack 101 is formed on the left side of the substrate 11. A source region 20 is formed in the substrate 11. A gate stack 22 is formed on the left side of the source region 20. A gate stack 30 is formed on the right side of the source region 20. A contact 30c is formed on the left side of the source region 20. Arrows S1, S2, and S3 indicate electrical connections from an external source to the source region 20 and the gate stacks 22 and 30.

The diagram shows the internal components of the electronic device 305. A dashed line separates the device from the external components. Inside, a micro-computer 401 is connected to an LCD controller 402 and a signal processing circuit 403. The micro-computer 401 receives data Dp from an external device and outputs Ssd to the signal processing circuit 403. The LCD controller 402 receives control signals Sv and Sp from the micro-computer 401 and outputs S1~S3 to the LCD module 205. The signal processing circuit 403 performs phase and amplitude control and D/A conversion, receiving Ssd from the micro-computer 401 and outputting S1~S3 to the LCD module 205.

Fig. 16

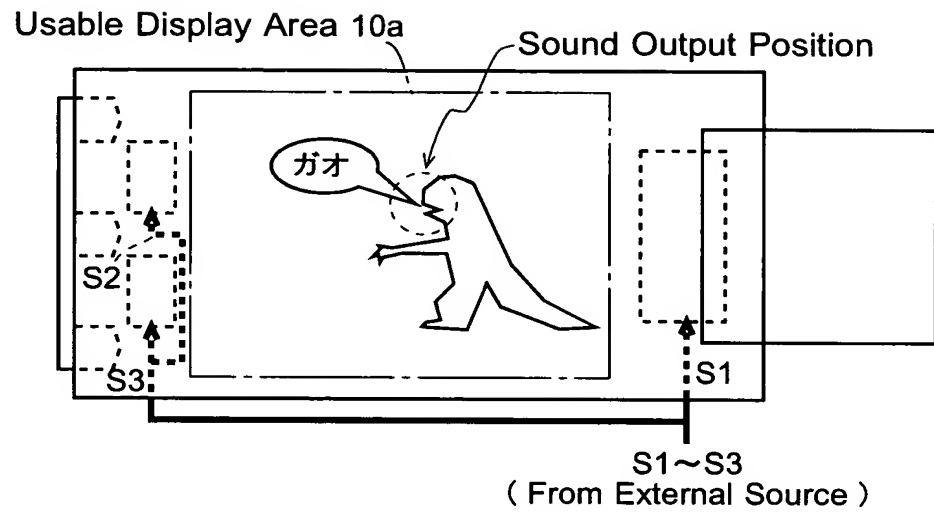
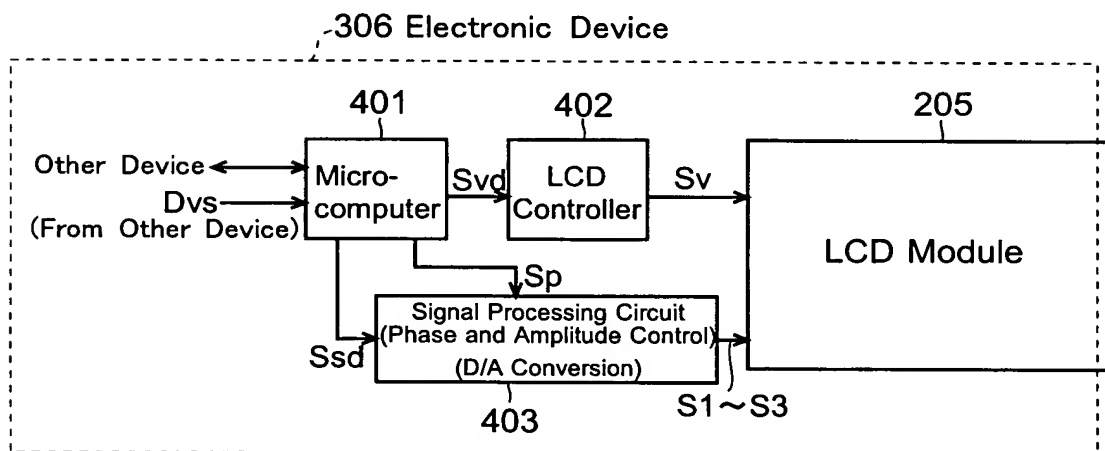


Fig. 17



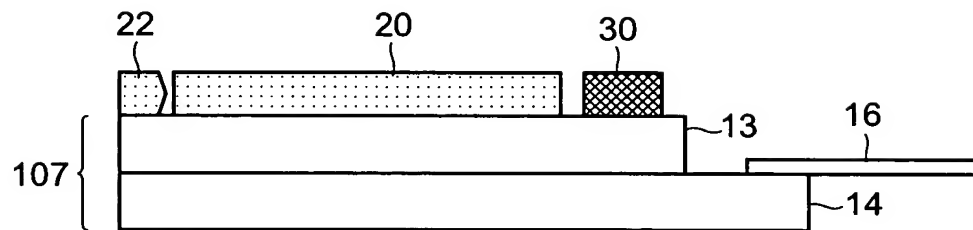
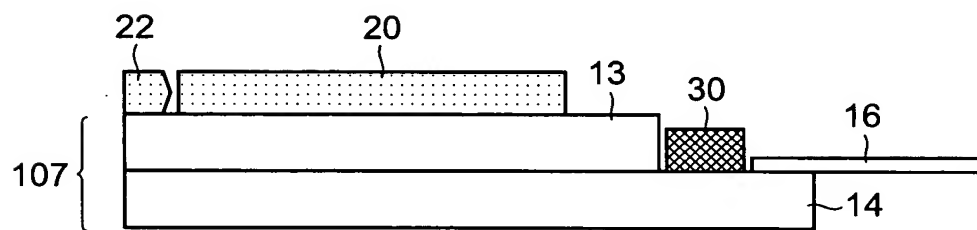
*Fig. 18**Fig. 19*



Fig.20

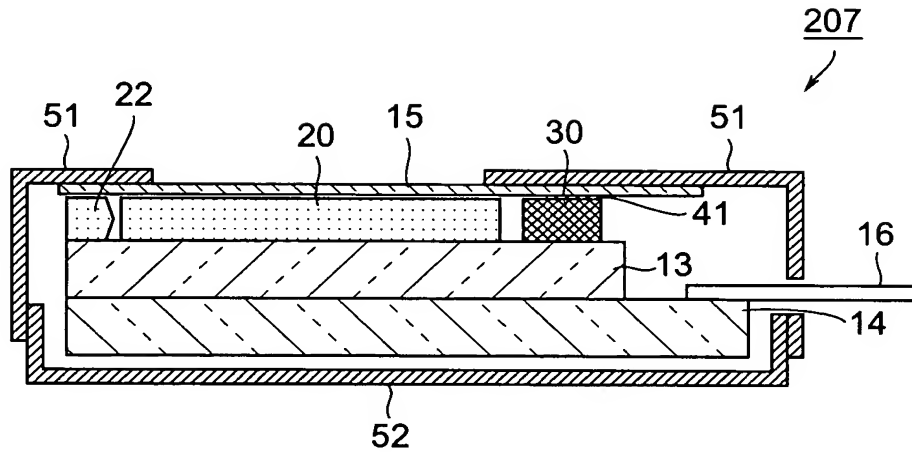
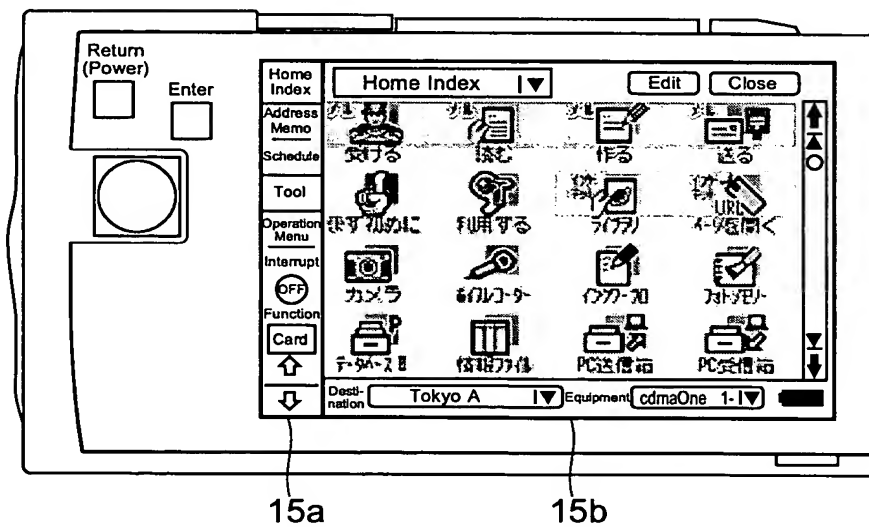
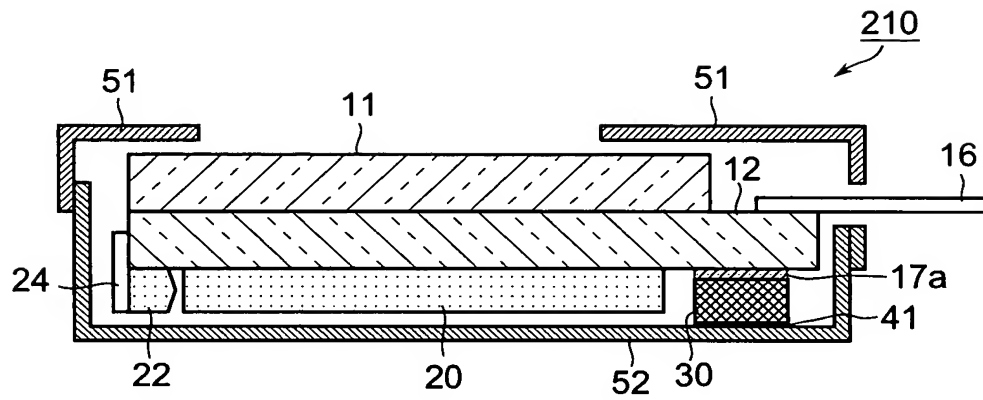
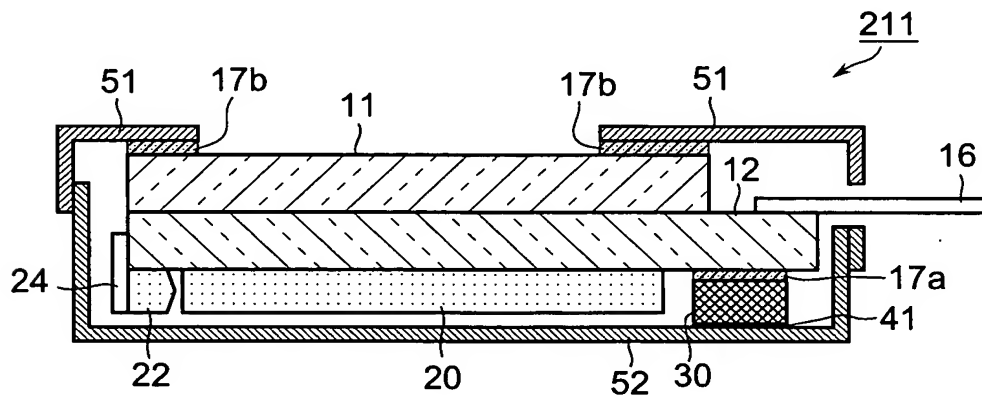
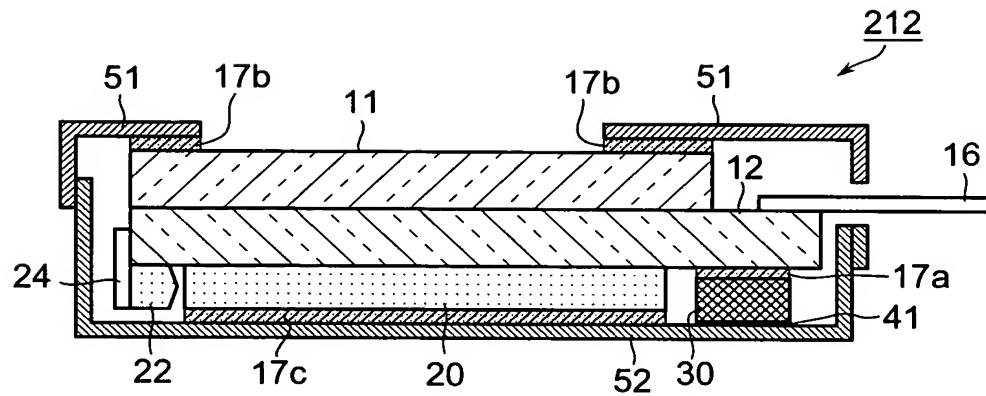
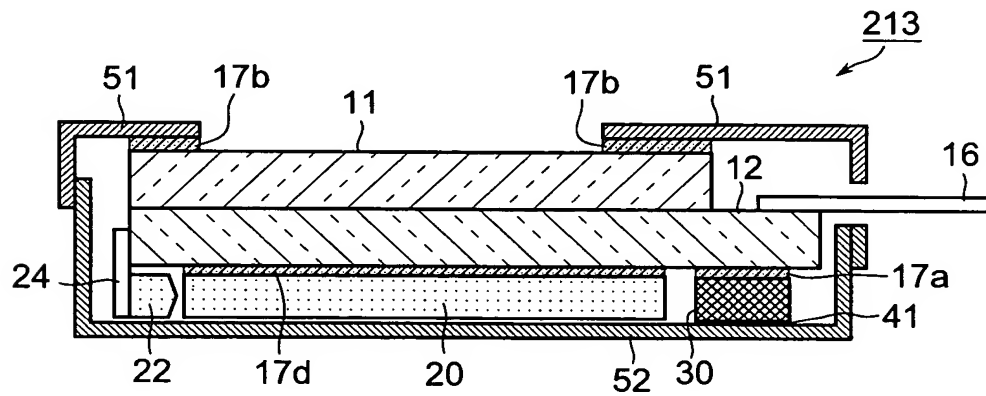
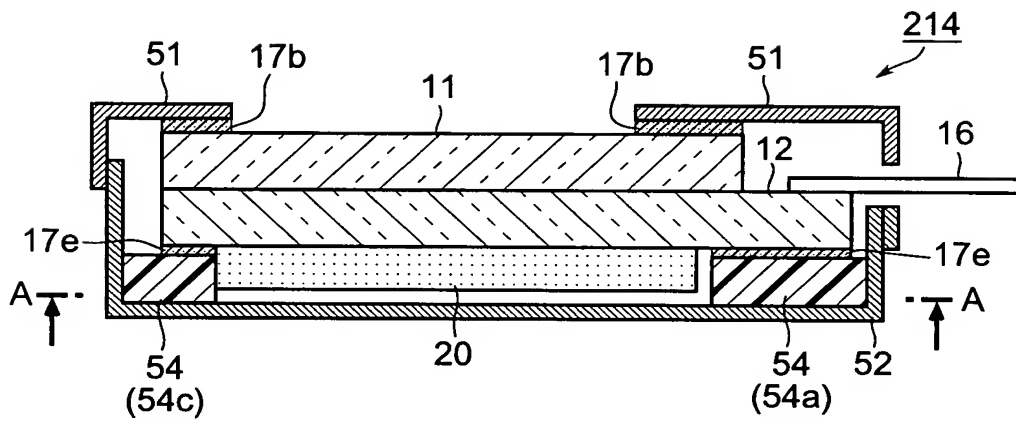
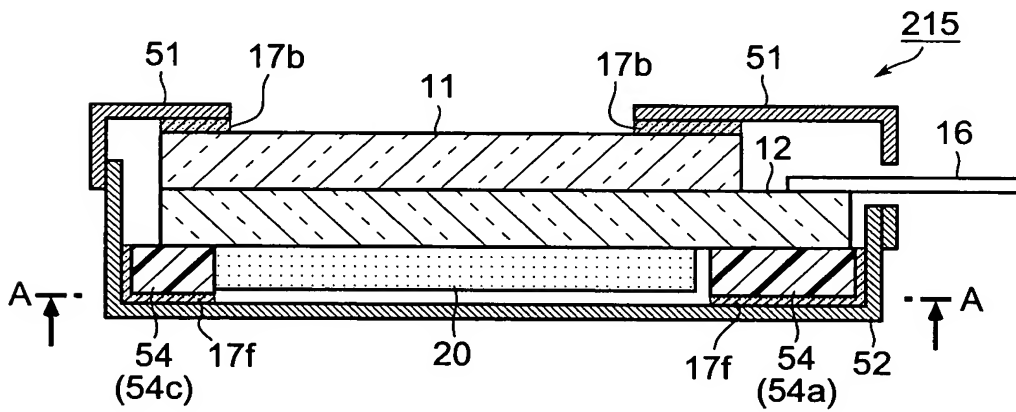


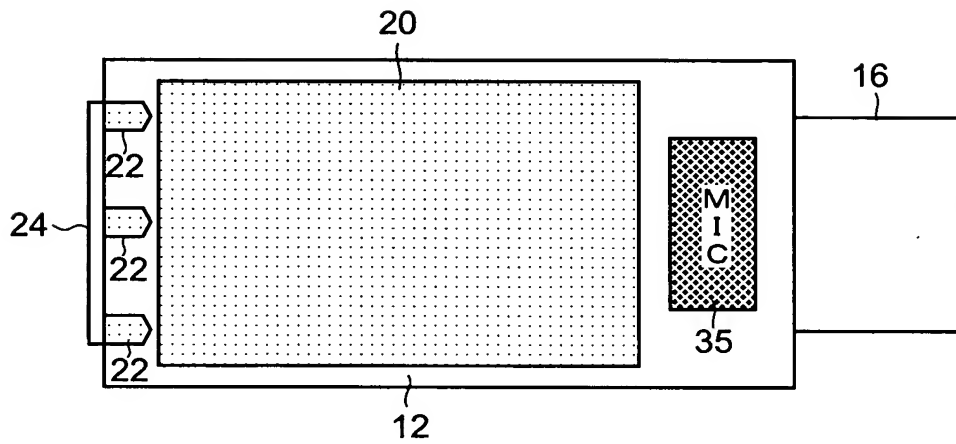
Fig.21



*Fig.22**Fig.23*

*Fig.24**Fig.25*

*Fig.26**Fig.27*

*Fig.28**Fig.29*